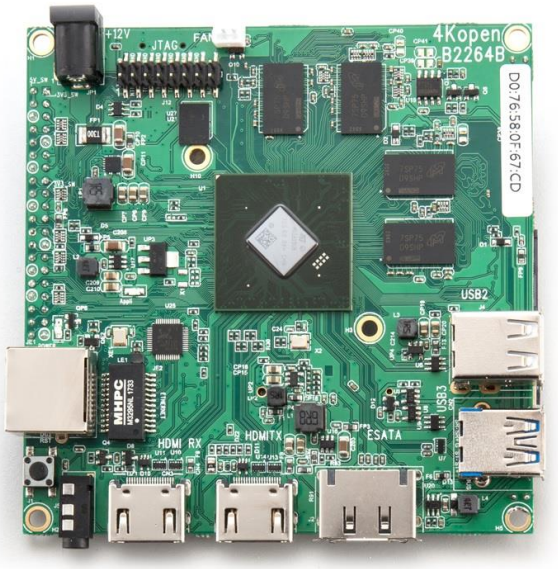
4kOpen Board Datasheet



Introduction

The purpose of this document is to describe the HW of 4K UltraHD H.265 / HEVC community board based on STiH418 for the 4kOpen platform.

The reference number of the 4kOpen board is B2264. The letter after B2264 indicates the version of the board PCB. For example, B2264B is the second board revision of the B2264.

Scope

This document is targeted at the following audiences in the context of 4kOpen project:

- Developers of HW platform similar to 4kOpen with STiH418
- Developers of SW for 4kOpen platform

Reference documentation

Below is a list of documents that should be consulted alongside the present document.

Table 1 References

#	Document name	Document description
[1]	STiH418 datasheet	Datasheet of the SOC

Acronyms and Abbreviations

B2264	4kOpen reference board
DCPS	Deep Controller Passive Standby
DeCap	Decoupling Capacitor
HDK	Hardware Development Kit
HW	Hardware
IR	Infrared Red receiver for remote control
N/A	Not Applicable
NC	Not Connected
MAC	Medium Access Control
SBC	Stand By Controller of the SOC
SOC	System On Chip (STiH418)
SW	Software
TS	Transport Stream from Digital Video Broadcast standard

Contents

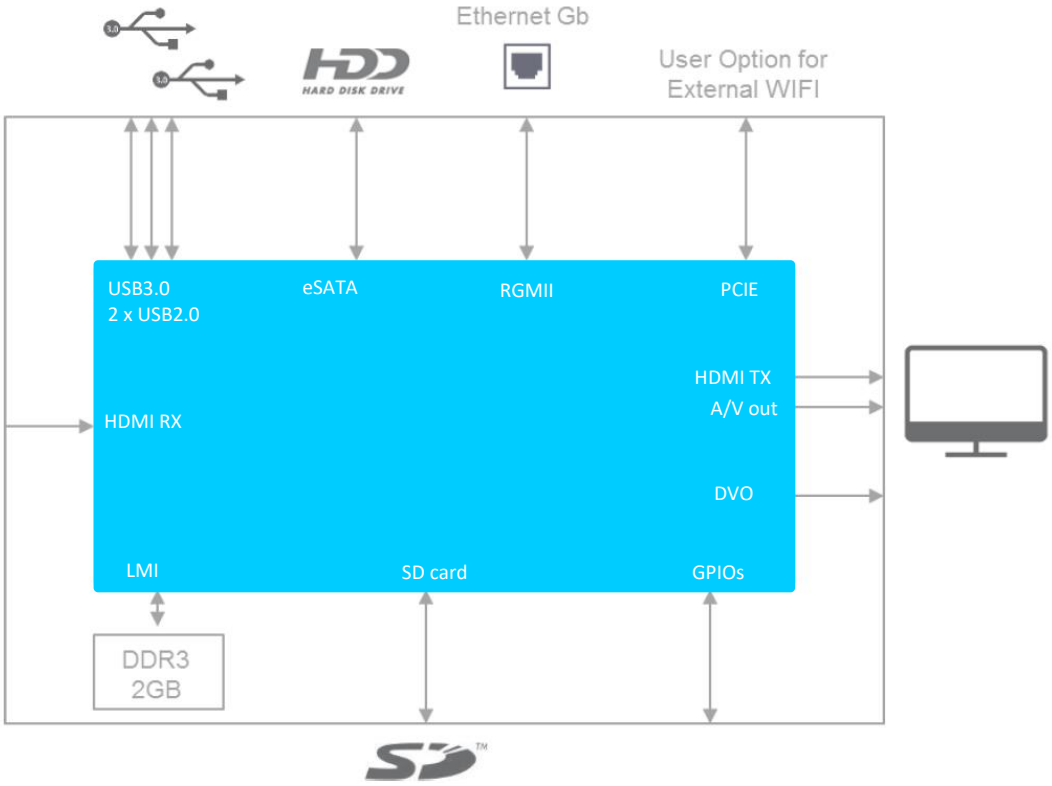
1 Platform description

1.1 Features

Function	Description
Main SOC	STiH418
DDR	2GBytes DDR3 2133 (4x4Gb 16bits)
DVO	yes
Touch screen interface	yes
SP-DIF	yes
HDMI out	1x
HDMI In	1x
Audio/video jack	1x
USB	1 x USB 3.0 2 x USB2.0
eSATA	1x
Ethernet	Gb PHY
Wi-Fi	Module on Mini PCIe connector
SD card	yes
On board supply	Yes
PCB	4 layers FR4 100x100mm

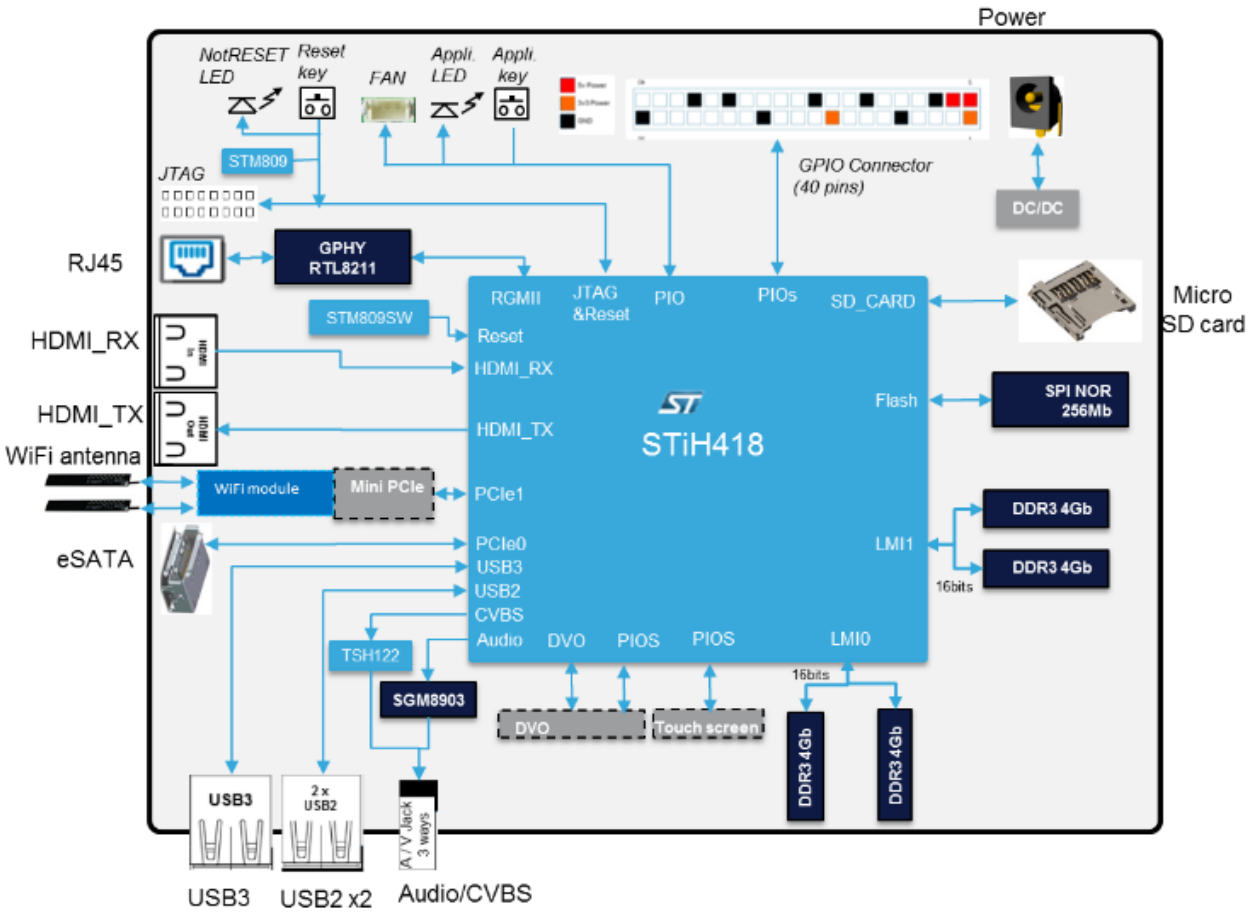
1.2 Board Overview

Figure 1: 4kOpen board overview



1.3 Block Diagram

Figure 2: 4kOpen block diagram of the board



2 Feature Description

- Main SOC
  - STiH418
- DDR
  - 2GB DDR3 2133 (4x4Gb 16bit)
- Flash
  - 1 SPI NOR 256Mbits
  - 1 Micro SD CARD
- Ethernet 1Gbits
  - RTL8211 phy (RJ45)
  - Wake-up on LAN
- External connectors
  - Micro SD card
  - 40 pins GPIO
  - HDMI RX
  - HDMI TX
  - eSATA
  - Mini PCIe
  - DVO + touch screen
  - Ethernet 1Gbits (RJ45)
  - USB3 X1
  - USB2 x2
  - JTAG
  - Audio/CVBS (Jack)
  - Fan control and connector
  - Power plug (jack)
- Mode pin selection :
  - Fixed by SMD resistors
- Led indicator
  - 1 red led power and reset not (based on signal SYS_AO_NOTRESETIN)
    - on when the SOC is functional
    - off when the SOC is in reset
  - 1 green led controlled by on PIO1[3] (application)
    - on when PIO1[3] is output low
    - off when PIO1[3] is output high
  - 2 RJ45 led controlled by the RTL8211
  - 2 led controlled by the Mini PCIe module
- Power supply
  - +7V to +12V power plug (Jack)
  - AVS for Vcore and Vcpu
  - Standby mode SBC wake –up (for power saving)
  - Switch on powering the Ethernet phy (for Power On line wake-up)
- PCB
  - FR4, 4 Layers target 450µm via diameter 100/100 µm line spacing, 1.6mm thickness
- Mechanics
  - PCB Size : 100x100mm

3 PCB View

3.1 PCB 4kOpen top and bottom view

Figure 3: 4kOpen PCB top view

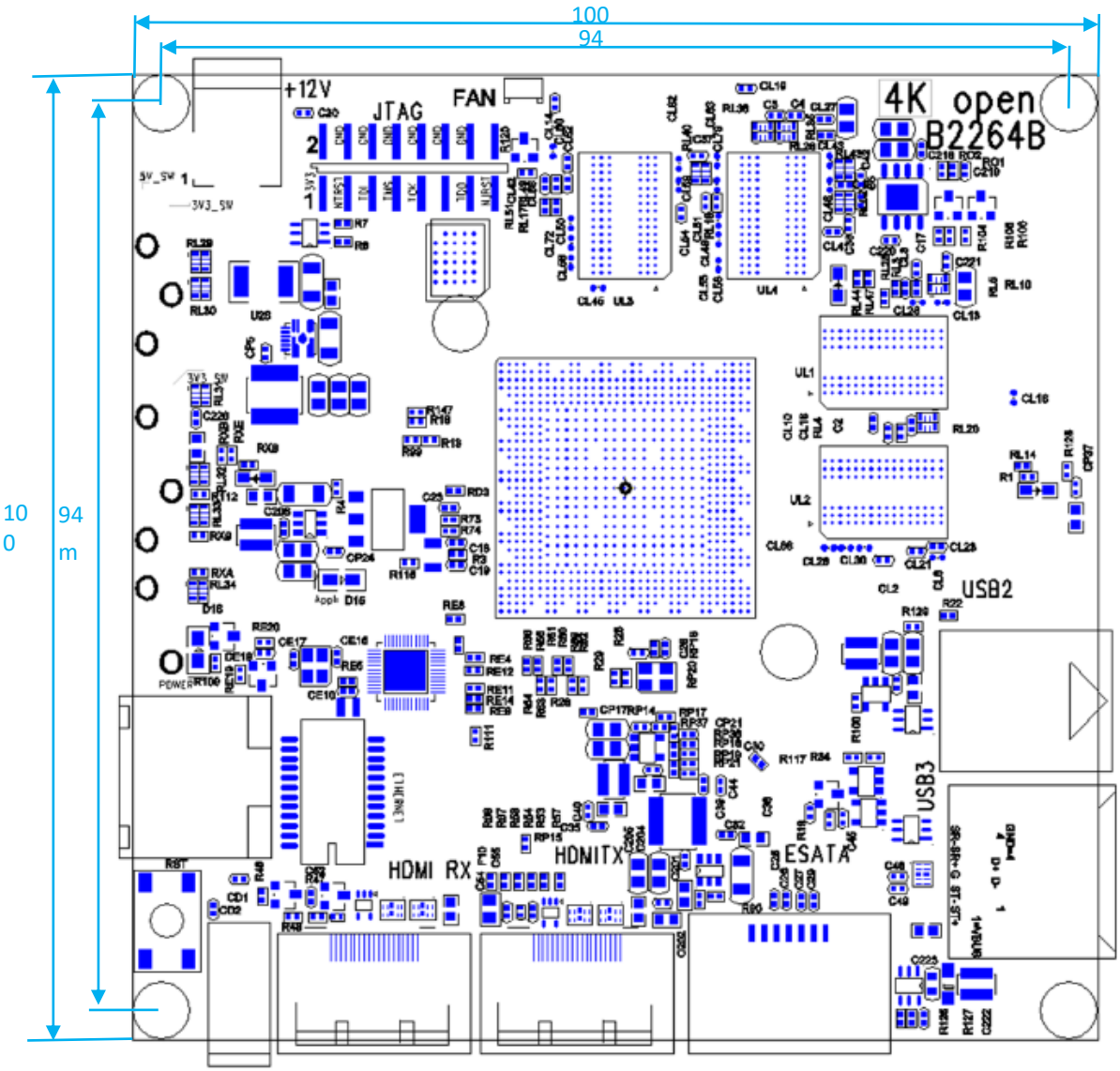
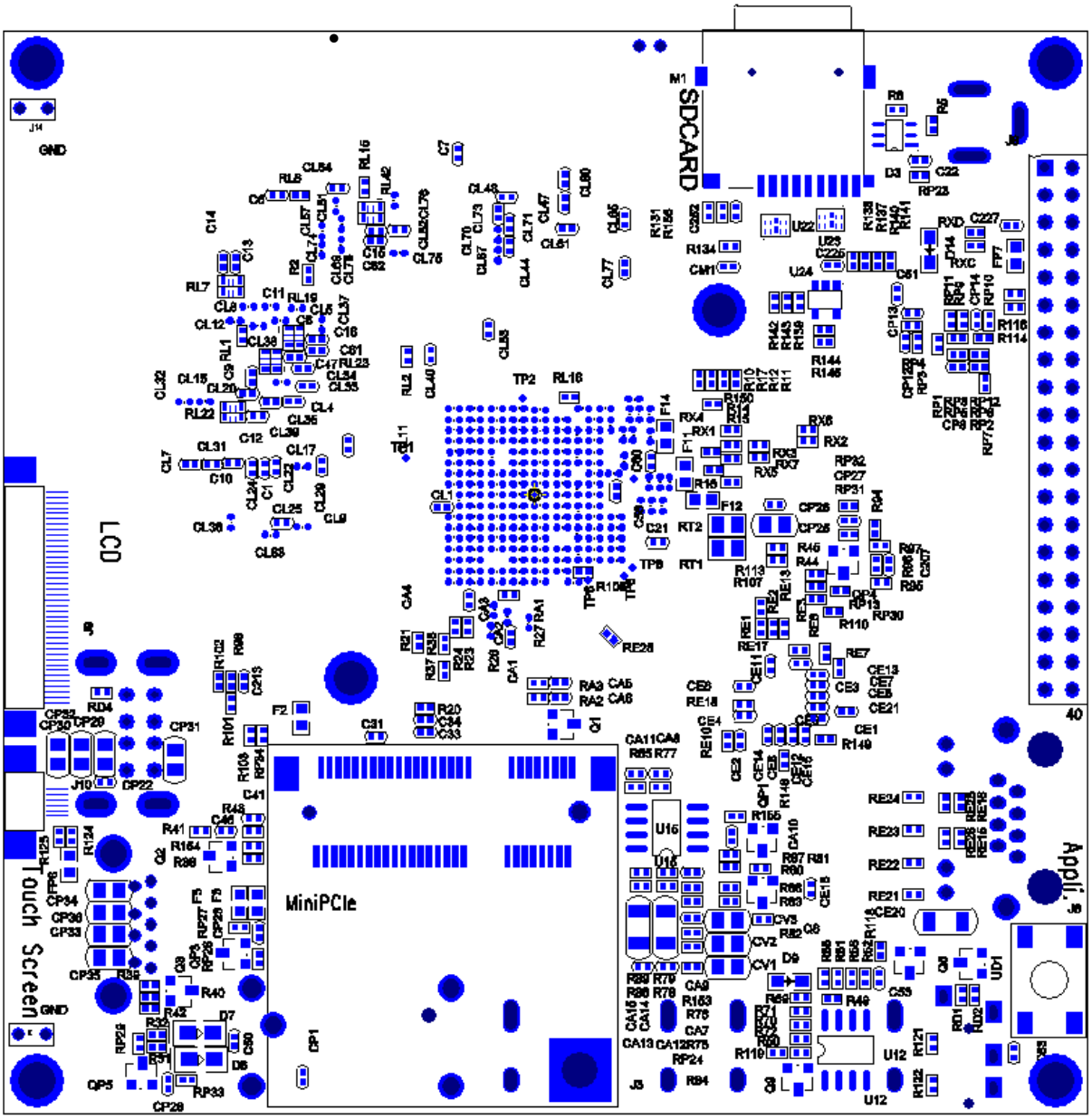


Figure 4: 4kOpen PCB bottom view



3.2 PCB Layers

Figure 5: 4kOpen Layer 1 (signals)

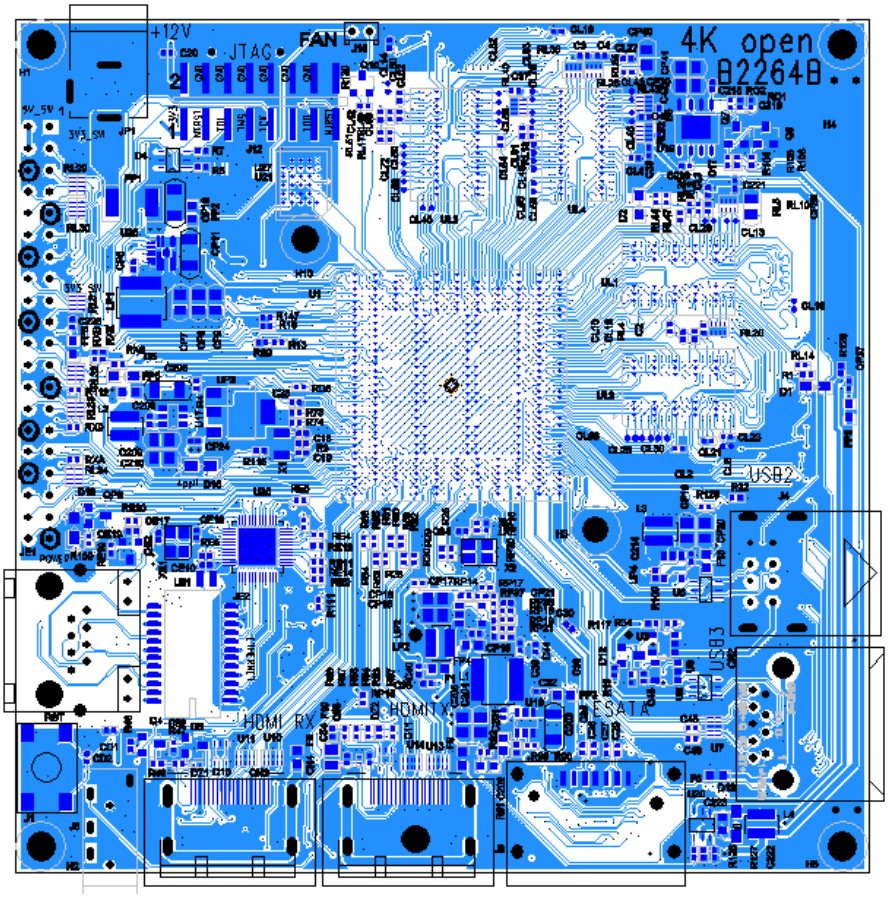


Figure 6: 4kOpen Layer 2 (ground)

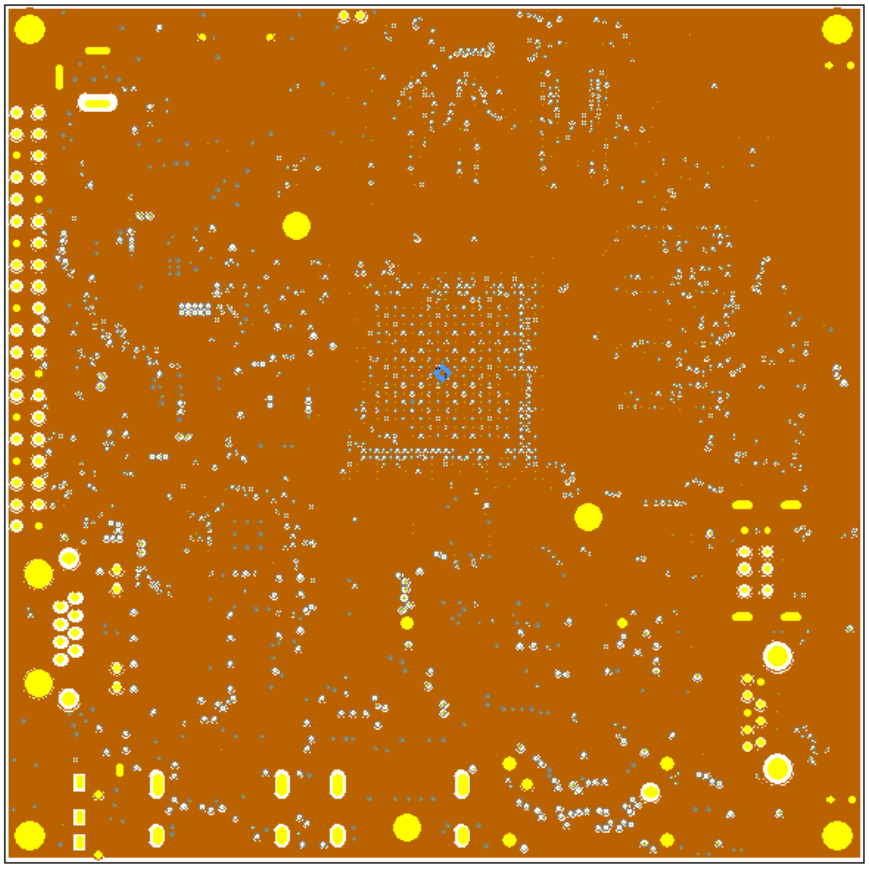


Figure 7: 4kOpen Layer 3 (power)

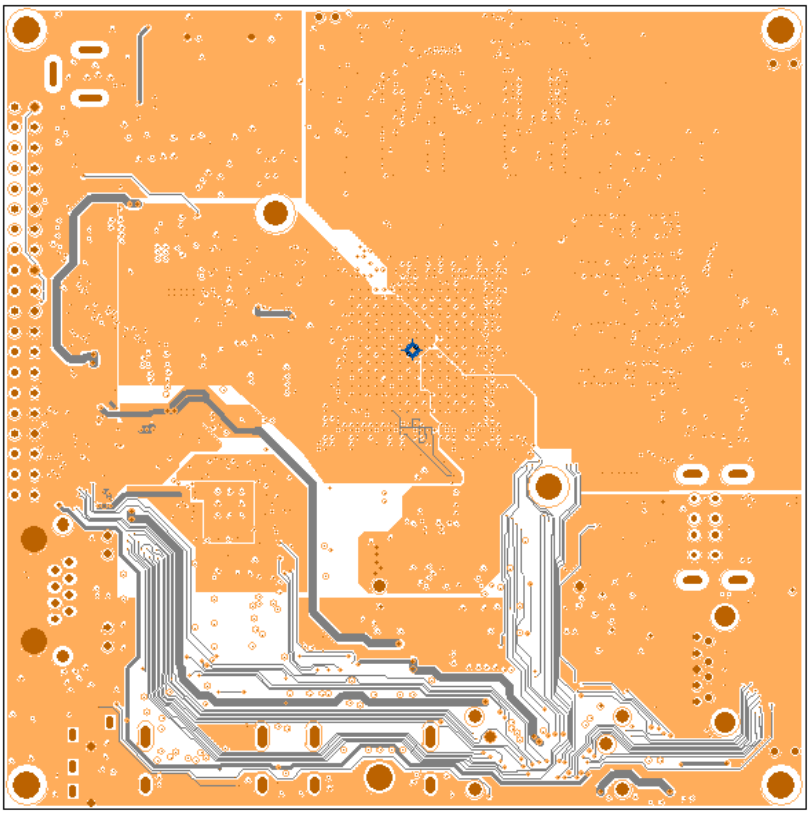
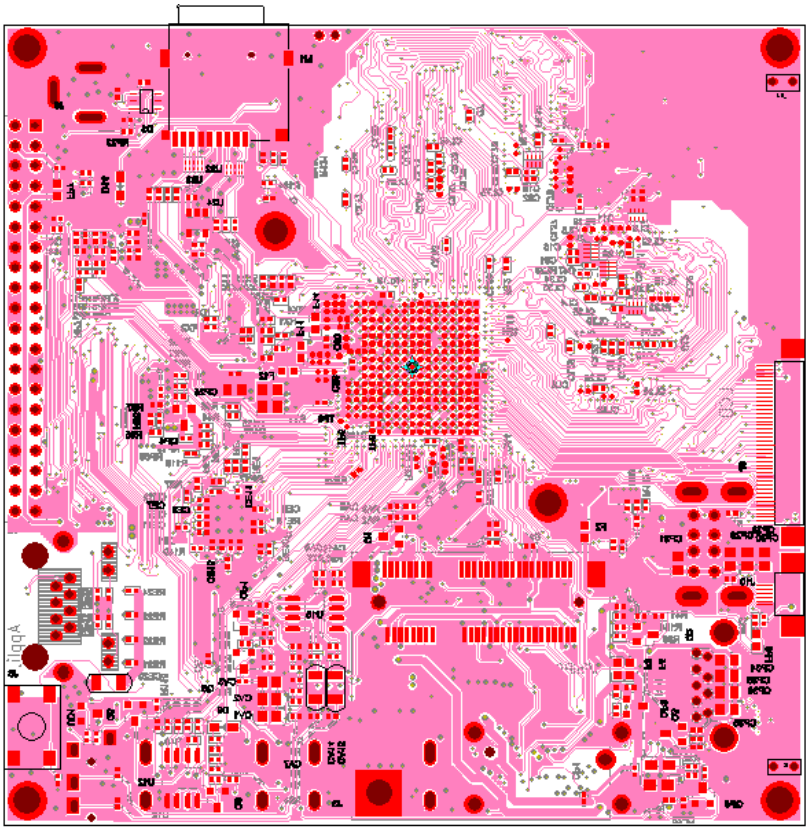
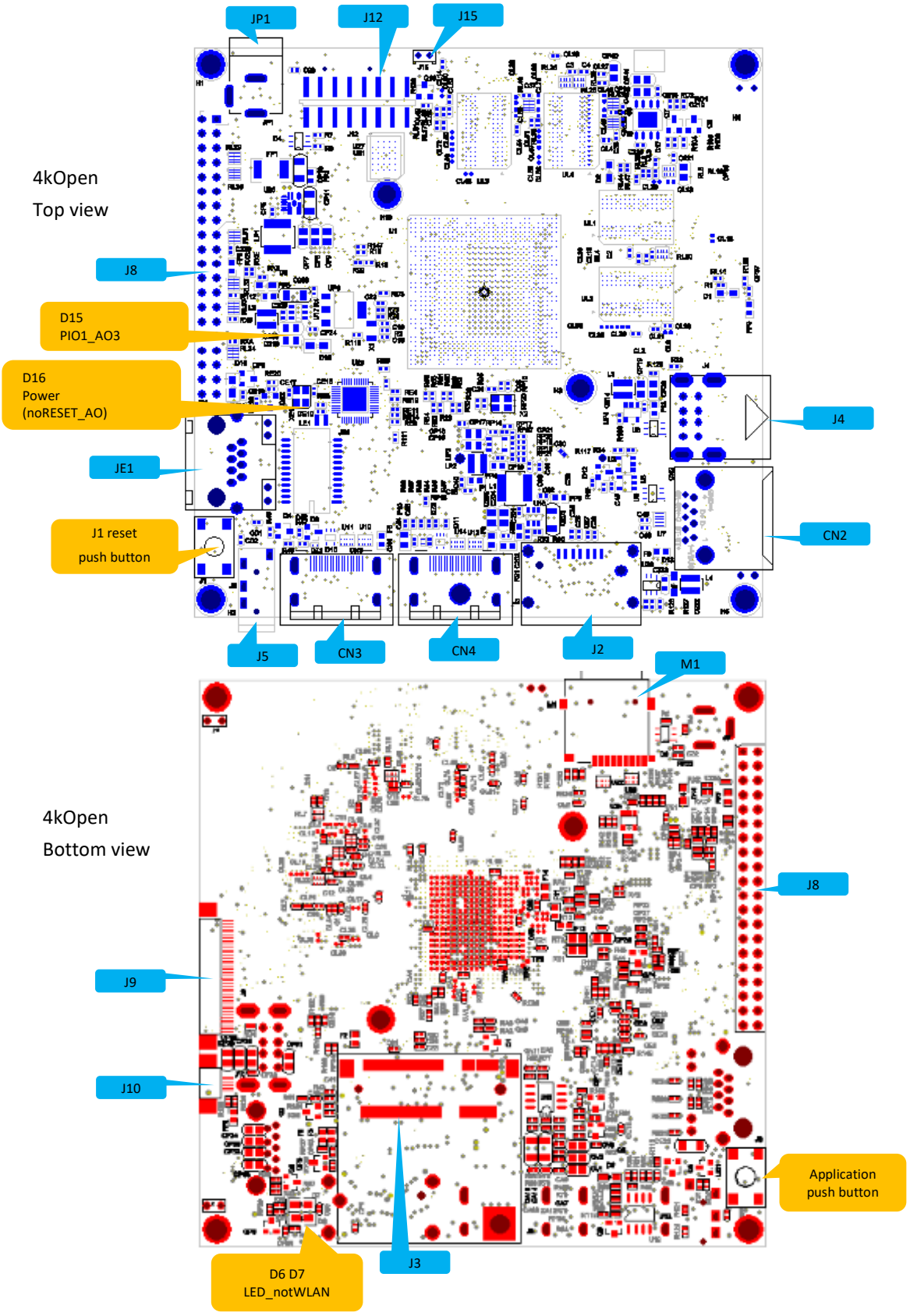


Figure 8: 4kOpen Layer 4 (signals)



4 Interfaces and connectors

Figure 9: Interfaces and connectors position



4.1 DC Power Connector (JP1)

A standard jack connector provides an interface connection for +12V DC input.

- Jack socket connector
- 5.5mm outer diameter
- 2.1mm inner diameter

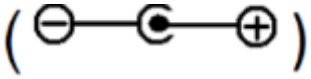


Figure 10: DC power socket

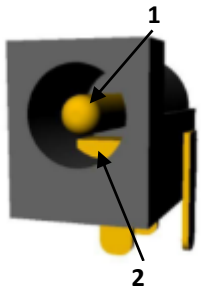


Table 2: DC power socket

Pin	Description	Signal direction	Pin	Description	Signal direction
1	+Vin	+12v DC to board	2	Ground	N/A

4.2 USB 2.0 Type A connector (J4)

A standard 4-pin USB Type A (Host) connector provides an interface connection for both USB1.1 and USB2.0 versions.

Figure 11: USB2.0 Type A connector

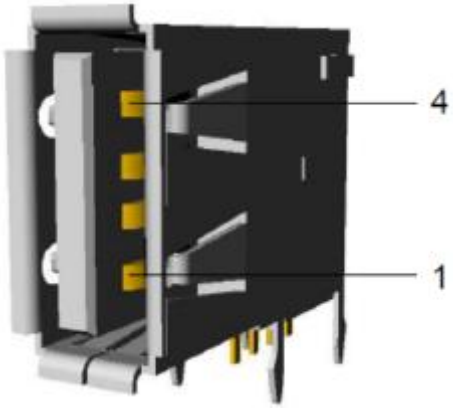


Table 3: USB Type A connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	VBUS	N/A	3	DP	Bi-Directional
3	DM	Bi-Directional	4	GROUND	N/A

4.3 USB 3.0 Type A connector (CN2)

A standard 9-pins USB 3.0 Type A (Host) connector provides an interface connection for USB 3.0 version.

Figure 12: USB 3.0 Type A connector

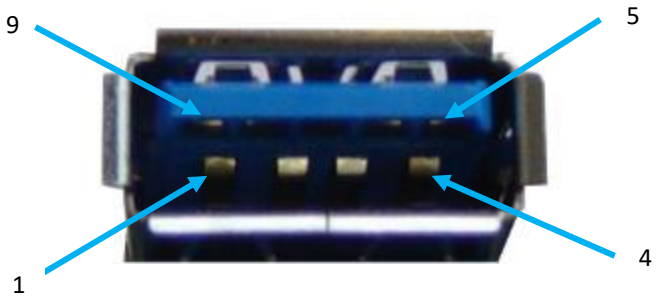


Table 4: USB3.0 Type A connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	VBUS	N/A	6	USB3RXP	To SOC
2	USB2_DM	Bi-Directional	7	GROUND	N/A
3	USB2_DP	Bi-Directional	8	USB3TXM	From SOC
4	GROUND	N/A	9	USB3TXP	From SOC
5	USB3RXM	To SOC			

4.4 CVBS/audio connector (J5)

A 4-pin CVBS/audio connector provides an interface connection for analog audio and video signals.

Figure 13: CVBS/audio connector

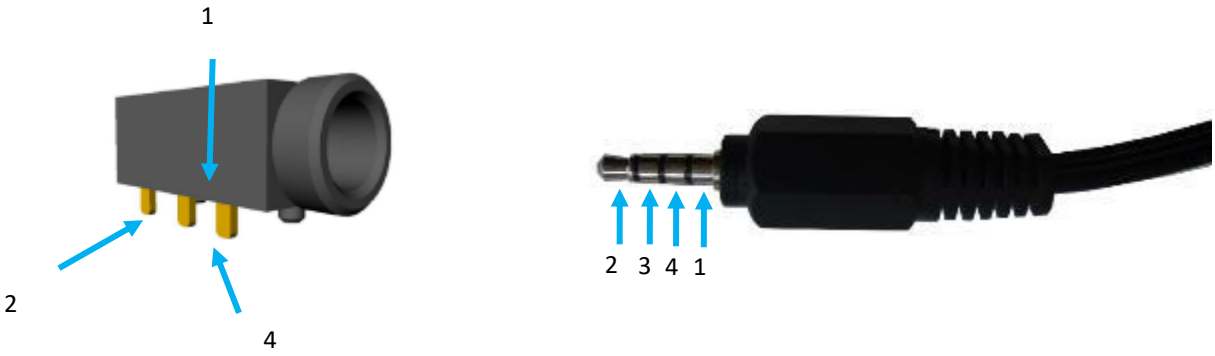


Table 5: CVBS/audio connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	GROUND	N/A	3	LEFT_OUT	From SOC
2	CVBSOUT	From SOC	4	RIGHT_OUT	From SOC

4.5 HDMI connectors (CN3 , CN4)

A standard two male, 19-pin connector provides an interface connection for HDMI output and input. CN4 is used for HDMI OUT and CN3 is used for HDMI IN.

This high-definition multimedia interface is a trademark of Licensing, LLC (associated license has to be taken separately by the board owner).

Figure 14: HDMI connector

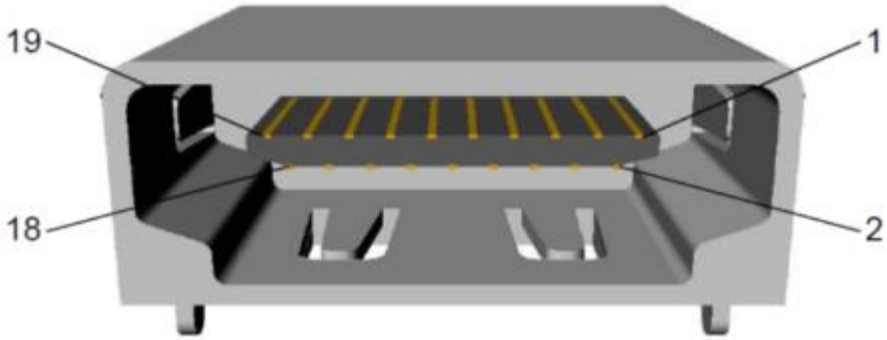


Table 6: HDMI connector (output) pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	TX2P	From SOC	11	GROUND	N/A
2	GROUND	N/A	12	TX_CLKN	From SOC
3	TX2N	From SOC	13	TX_CEC	Bi-Directional
4	TX1P	From SOC	14	NC	N/A
5	GROUND	N/A	15	TX_SCL	From SOC
6	TX1N	From SOC	16	TX_SDA	Bi-Directional
7	TX0P	From SOC	17	GROUND	N/A
8	GROUND	N/A	18	+5V_HDMI_TX	N/A
9	TX0N	From SOC	19	TX_HPD	To SOC
10	TX_CLKP	From SOC			

Table 7: HDMI connector (input) pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	RX2P	To SOC	11	GROUND	N/A
2	GROUND	N/A	12	RX_CLKN	To SOC
3	RX2N	To SOC	13	RX_CEC	Bi-Directional
4	RX1P	To SOC	14	NC	N/A
5	GROUND	N/A	15	RX_SCL	To SOC
6	RX1N	To SOC	16	RX_SDA	Bi-Directional
7	RX0P	To SOC	17	GROUND	N/A
8	GROUND	N/A	18	+5V_HDMI_RX	N/A
9	RX0N	To SOC	19	RX_HPD	To SOC
10	RX_CLKP	To SOC			

4.6 microSD Card Connector (M1)

A 15-pin, microSD card connector provides an interface connection micro SD card.

Figure 15: TF card connector

Table 8: TF card connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	DATA2	Bi-Directional	9	SDCARD_DETECT	To SOC
2	DATA3	Bi-Directional	10	GROUND	N/A
3	CMD	From SOC	11		
4	VDD	N/A	12		
5	CLK	From SOC	13		
6	GROUND	N/A	14	NC	N/A
7	DATA0	Bi-Directional	15		
8	DATA1	Bi-Directional			

4.7 Ethernet Connector (JE1)

An RJ45 connector provides a 1000 BaseT Ethernet physical layer (PHY) interface.

Figure 16: Ethernet connector

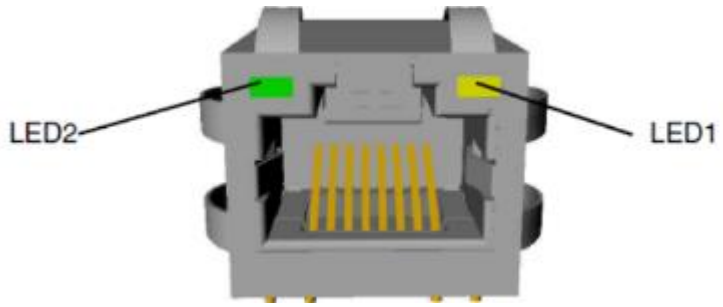


Table 9: Ethernet connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	PHY_DA+	Bi-Directional	9	LEDY+	LED Anode
2	PHY_DA-	Bi-Directional	10	LEDY-	LED Cathode
3	PHY_DB+	Bi-Directional	11	LEDG+	LED Anode
4	PHY_DC+	Bi-Directional	12	LEDG-	LED Cathode
5	PHY_DC-	Bi-Directional	15	GROUND	N/A
6	PHY_DB-	Bi-Directional	16	GROUND	N/A
7	PHY_DD+	Bi-Directional			
8	PHY_DD-	Bi-Directional			

4.8 Mini PCIe Connector (J3)

A standard Mini PCIe connector provides an interface connection for Mini PCIe module. The 4kOpen board supports half size module. Nevertheless a full size module can be plug on 4kOpen board without screw fixation

Figure 17: PCI-e connector

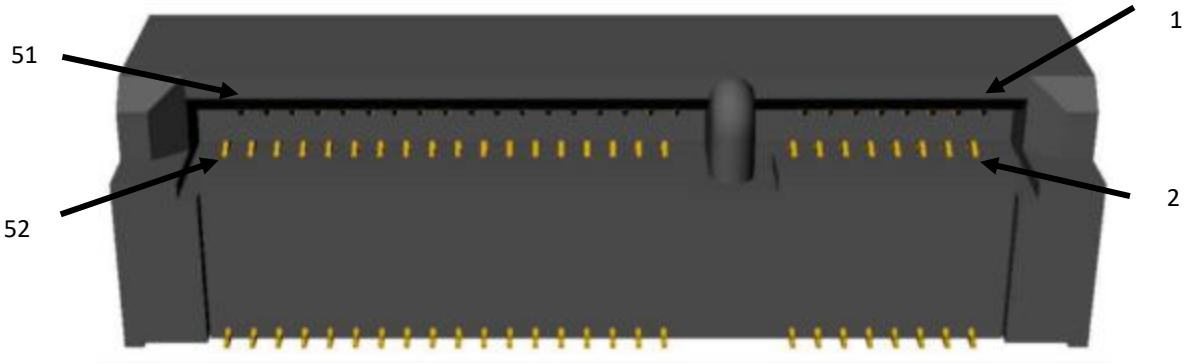


Table 10: PCI-e connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	WAKEnot	To SOC	2	3V3_PCIe	N/A
3	NC	N/A	4	GND	N/A
5			6	+1V5	N/A
7			8	NC	N/A
9	GND	N/A	10		
11	PCIE_CLKN	From SOC	12		
13	PCIE_CLKP	From SOC	14		
15	GND	N/A	16		
17	NC	N/A	18	GND	N/A
19			20	NC	N/A
21	GND	N/A	22	PCIE_RSTN	From SOC
23	PCIE_RXN	To SOC	24	3V3_PCIe	N/A
25	PCIE_RXP	To SOC	26	GND	N/A
27	GND	N/A	28	+1V5	N/A
29			30	SSC5_SCL	From SOC
31	PCIE_TXN	From SOC	32	SSC5_SDA	From SOC
33	PCIE_TXP	From SOC	34	GND	N/A
35	GND	N/A	36	NC	N/A
37			38		
39	3V3_PCIe	N/A	40	GND	N/A
41			42	NC	N/A
43	GND	N/A	44	LED_notWLAN	From module
45	NC	N/A	46	LED_notWPAN	From Module
47			48	+1V5	N/A
49			50	GND	N/A
51			52	3V3_PCIe	N/A

4.9 eSATA Connector (J2)

A standard sSATA connector provides an interface connection for an external SATA module.

Figure 18: eSATA connector

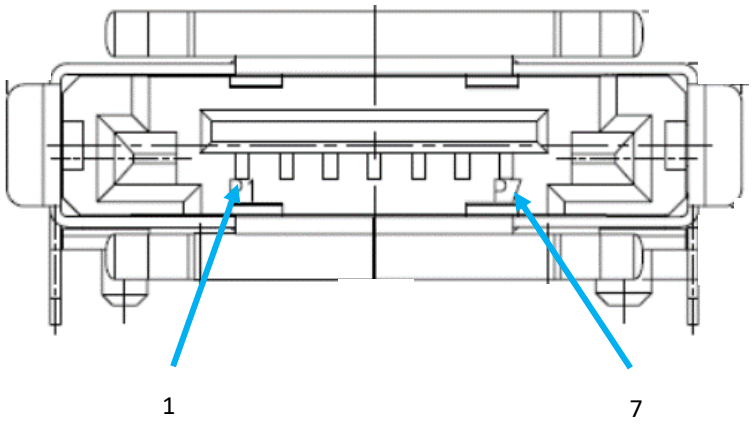


Table 11: eSATA connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	GROUND	N/A	8	GROUND	N/A
2	TX+	From SOC	9		
3	TX-	From SOC	10		
4	GROUND	N/A	11		
5	RX-	To SOC			
6	RX+	To SOC			
7	GROUND	N/A			

4.10 GPIO 40 Pins Connector (J8)

A 40 pins male connector 2.54mm pitch provides an interface connection for an application module with 3V3 and 5V supply and many GPIOs.

Figure 19: 40 pins GPIO connector (Bottom PCB view)

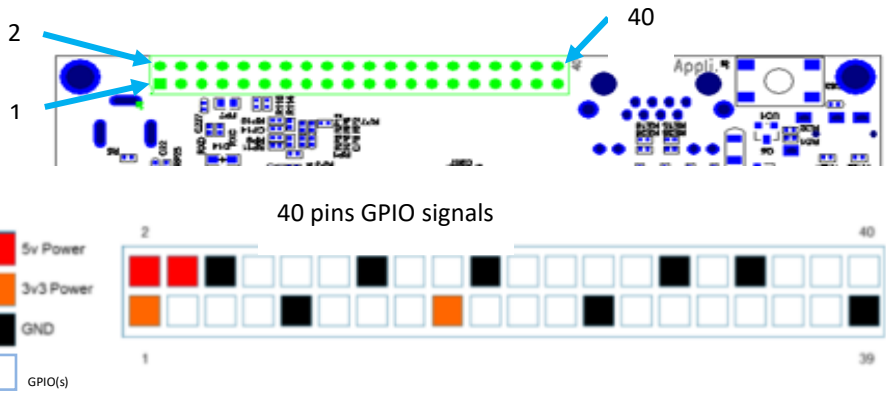


Table 12: 40 pins GPIO connector pin allocation

Pin	Description	Comment	Alternate 1	Alternate 2	Alternate 3	Alternate 4	Alternate 6
1	3V3_SW	Switched supply					
2	5V_SW	Switched supply					
3	PIO4[6]		SSC10_MTSR	TRIGGER_OUT	PWM12_OUT	KEY_SCAN_OUT[0]	
4	5V_SW	Switched supply					
5	PIO4[5]		SSC10_SCL	TRIGGER_IN		KEY_SCAN_IN[1]	
6	GROUND	N/A					
7	PIO4[4]		PWM11_OUT		SBC_OBS_NOTRST	KEY_SCAN_IN[0]	
8	PIO3[4]		UART10_TXD	SSC12_MRST			
9	GROUND	N/A					
10	PIO3[5]		UART10_RXD	ACG_CLK_OBS0			
11	PIO2[7]			KEY_SCAN_OUT[3]	UART11_RXD	MII1_TXD[5]	
12	PIO34[7]		AUDSPDIF_OUT	AUDPCMIN0_DATA[1]	clockgen_d_11_obs_0	UART3_NOT_OE	
13	PIO2[6]			KEY_SCAN_IN[3]	UART11_TXD	MII1_TXD[4]	
14	GROUND	N/A					
15	PIO0[6]		MII1_TXCLK	KEY_SCAN_OUT[2]	SBC_SYS_CLK_IN_ALT	ACG_CLK_OBS1	LPM_TESTBUS_0_[6]
16	PIO33[4]		AUDPCMOUT0_DATA[0]			clockgen_d_10_obs_0	
17	3V3_SW	Switched supply					
18	PIO33[5]		AUDPCMOUT0_MCLK				
19	PIO34[1]		AUDPCMOUT0_DATA[2]	AUDPCMIN0_SCLK	SSC4_MTSR	UART3_RXD	
20	GROUND	N/A					
21	PIO34[2]		AUDPCMOUT0_DATA[3]	AUDPCMIN0_LRCLK	SSC4_MRST	UART3_CTS	
22	PIO33[6]		AUDPCMOUT0_SCLK	AUDPCMIN0_DATA[2]			
23	PIO34[0]		AUDPCMOUT0_DATA[1]	AUDPCMIN0_MCLK	SSC4_SCL	UART3_TXD	
24	PIO34[6]		EXT_IT[5]	AUDPCMIN0_DATA[0]	clockgen_d_10_obs_1	UART3_RTS	
25	GROUND	N/A					
26	PIO3[3]		FP_RESETN		EXT_IT[2]		
27	PIO14[6]		SSC2_MTSR		TSIN4_DATA[7]		
28	PIO14[5]		SSC2_SCL		TSIN4_BYTECLK		
	PIO13[6]		TSIN3_VALID	TSIN2_DATA[5]	SSC3_MTSR	EXT_DMA_REQ0	
29	PIO4[0]		UART10_NOT_OE	IRB10_IR_IN			
	PIO4[2]		PWM11_COMPAREOUT	IRB10_IR_DATA_OUT		MII1_TXD[7]	KEY_SCAN_OUT[0]
30	GROUND	N/A					
31	PIO4[1]			IRB10_UHF_IN		MII1_TXD[6]	KEY_SCAN_IN[1]
	PIO4[3]		PWM11_CAPTUREIN		EXT_IT[3]	MII1_PHY_REF_CLK	KEY_SCAN_OUT[1]
32	PIO17[3]		UART0_RTS	SC0_NOT_SET_VPP	MCHI_SCTL	ALT_PHY_TDO	
	PIO16[6]			SC1_C8_UART		clockgen_c_10_obs_0	SD_LED
33	PIO16[7]			SC1_DETECT		clockgen_c_10_obs_1	SD_PWREN
34	GROUND	N/A					
35	PIO14[4]		SSC1_MRST		TSIN4_PACKETCLK	MII1_RXD[7]	KEY_SCAN_IN[0]
	PIO13[7]		TSIN3_PACKETCLK	TSIN2_DATA[4]	SSC3_MRST	EXT_DMA_REQ1	
36	PIO17[2]		UART0_CTS	SC0_NOT_SET_VCC	MCHI_SCLK	ALT_PHY_TCK	
	PIO15[4]		UART2_NOT_OE	NMI	DVBCI_ADDR[10]	TPIU_DATA[12]	
37	PIO33[7]		AUDPCMOUT0_LRCLK	AUDPCMIN0_DATA[3]			
38	PIO14[3]		SSC1_MTSR	TSIN2_DATA[0]	TSIN4_VALID		
	PIO17[0]		UART0_TXD	SC0_C4_UART		clockgen_d_13_obs_0	
39	GROUND	N/A					
40	PIO14[2]		SSC1_SCL	TSIN2_DATA[1]	TSIN4_ERROR		
	PIO17[1]		UART0_RXD	SC0_C7_UART		clockgen_d_13_obs_1	

Color legend of “description” and “comments” columns of Table 12

Single GPIO signal connected

Dual GPIO signal connected. This is to allow further functionalities.

This means the application must manage the PIO configuration (input/output) accordingly to avoid HW conflict between separated PIO connected to the same pin.

There must not be simultaneously 2 PIOs connected together in push-pull output at the same time

SBC GPIO (PIO1/2/3/4/5 always on)

4.11 LCD Display Connector (J9)

A flat 40 pins flat connector provides an interface connection to a LCD display through DVO of the STiH418.
The DVO interface is 3*8 bits RGB.

Figure 20: 40 pins Display connector (bottom PCB view)

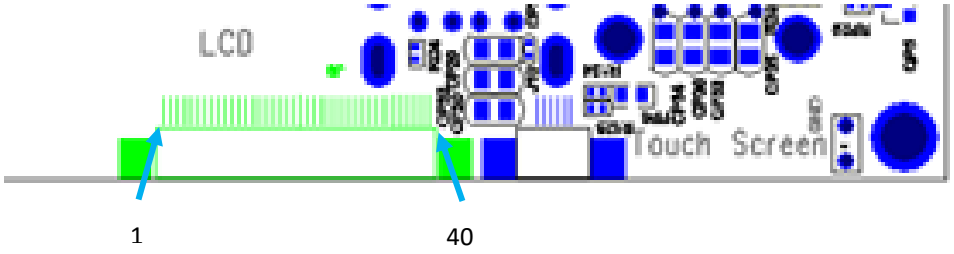


Table 13: LCD display connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	BL_LED-	From SOC	21	DVO_0	From SOC
2	BL_LED+	From SOC	22	DVO_1	From SOC
3	GROUND	N/A	23	DVO_2	From SOC
4	+3V3_SW	N/A	24	DVO_3	From SOC
5	DVO_16	From SOC	25	DVO_4	From SOC
6	DVO_17	From SOC	26	DVO_5	From SOC
7	DVO_18	From SOC	27	DVO_6	From SOC
8	DVO_19	From SOC	28	DVO_7	From SOC
9	DVO_20	From SOC	29	GROUND	N/A
10	DVO_21	From SOC	30	DVO_CK	From SOC
11	DVO_22	From SOC	31	LCD_DISP	From SOC
12	DVO_23	From SOC	32	DVO_HS	From SOC
13	DVO_8	From SOC	33	DVO_VS	From SOC
14	DVO_9	From SOC	34	DVO_DE	From SOC
15	DVO_10	From SOC	35	NC	
16	DVO_11	From SOC	36	GROUND	N/A
17	DVO_12	From SOC	37	LCD_RSTN	From SOC
18	DVO_13	From SOC	38	LCD_SDI	Bi-Directional
19	DVO_14	From SOC	39	LCD_SCL	From SOC
20	DVO_15	From SOC	40	LCD_CS	From SOC

4.12 Touch screen connector (J10)

A 6 pins flat connector provides an interface connection for a capacitive touch screen.

Figure 21: 40 pins Display connector (bottom PCB view)

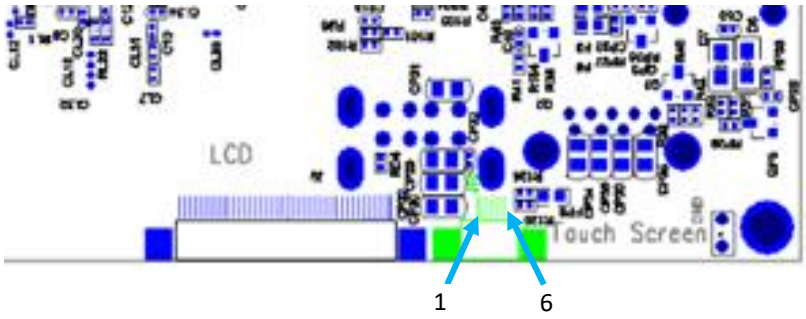


Table 14: Touch screen display connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	3V3_SW	N/A	4	SSC5_SCL	From SOC
2	LCDTS_RESET	From SOC	5	SSC5_SDA	Bi-Directional
3	LCDTS_INT	To SOC	6	GND	N/A

The Back light is delivered through a STLD40DPUR and enabled by a PIO.

4.13 Fan Connector (J15)

A 2 pins male connector 2.54mm provides an interface connection for a fan.

The fan is an option. it is controlled by a PIO.

Depending on the operating conditions and usage, the replacement of the provided heat think by a fan may be recommended. User have to check the operating junction temperature of the main chip in order to keep it in the specified range.

Table 15: 42 pins fan connector (top PCB view)

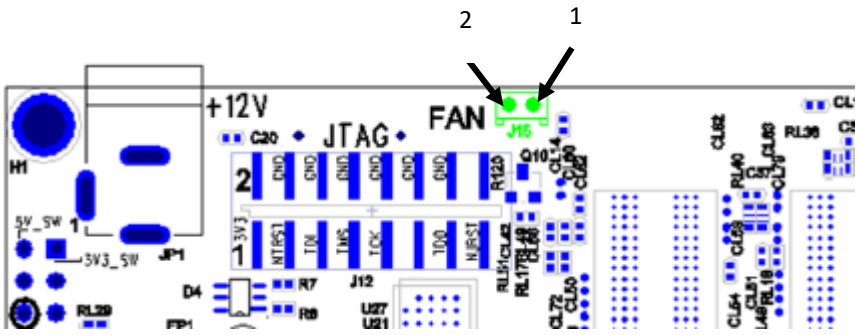


Table 16: FAN connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	+12V_SW	N/A	2	switch to ground	From SOC

4.14 JTAG Connector (J12)

A 16 pins male connector 2.54mm provides an interface connection for JTAG interface

Figure 22: JTAG connector (top view)

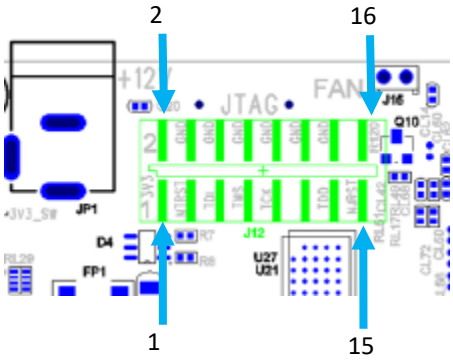


Table 17: JTAG connector pin allocation

Pin	Description	Signal direction	Pin	Description	Signal direction
1	3V3_JTAG	N/A	2	3V3_JTAG	N/A
3	JTAG_nTRST	To SOC	4	GROUND	N/A
5	JTAG_TDI	To SOC	6		
7	JTAG_TMS	To SOC	8		
9	JTAG_TCK	To SOC	10		
11	NC		12		
13	JTAG_TDO	From SOC	14		
15	JTAG_nJRST	To SOC	16		

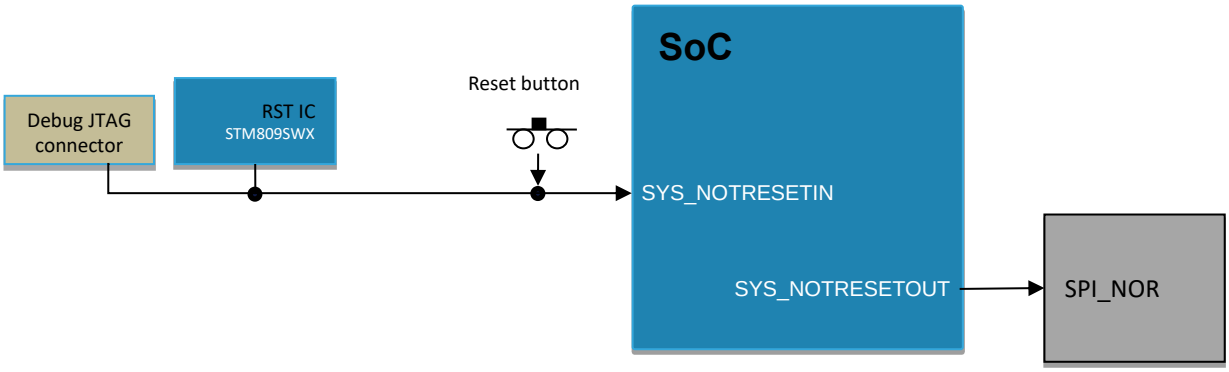
5 HW Description

5.1 SOC

The board is assembled with STiH418-DDUB from STMicroelectronics. See reference [1].

5.2 Reset & Boot

Figure 23: 4kOpen reset control path



5.3 Memory Interface

- SPI Flash 256Mbit
- Micro SD card through Micro SD connector

5.4 LMI Interface

- 2GB DDR3 2133 (4x4Gb 16bit)

5.5 PIOs

The table below lists all STiH418 PIOs with alternate function and the allocation on the 4kOpen board

Table 18: SOC GPIO

Partition	PIO pins	Alternate 1	Alternate 2	Alternate 3	Alternate 4	Alternate 5	Alternate 6	4kOpen board allocation
SBC	**PIO0**	**MII1, RMII1, GMII1, RevMII1**	**Key scanning, RevMII1**	**EXT_IT[1:0], Alternate clock input**	**ACG clk obs**			
	PIO0[0]	MII1_TXD[0]						RGMII
	PIO0[1]	MII1_TXD[1]						RGMII
	PIO0[2]	MII1_TXD[2]	KEY_SCAN_IN[0]					RGMII
	PIO0[3]	MII1_TXD[3]	KEY_SCAN_IN[1]					RGMII
	PIO0[4]	MII1_TXER	KEY_SCAN_IN[2]	EXT_IT[0]				RGMII
	PIO0[5]	MII1_TX_EN						RGMII
	PIO0[6]	MII1_TXCLK	KEY_SCAN_OUT[2]	SBC_SYS_CLK_IN_ALT				PIO0[6]
	PIO0[7]	MII1_COL	RevMII1_COL	EXT_IT[1]				M_RGMII1_notRESET
SBC	**PIO1**	**MII1, RMII1, GMII1, RevMII1**	**RevMII1, Key scanning**					
	PIO1[0]	MII1_MDIO						RGMII
	PIO1[1]	MII1_MDC	RevMII1_MDC					RGMII
	PIO1[2]	MII1_CRS	RevMII1_CRS					ETH_PEN
	PIO1[3]	MII1_MDINT						POW_LED_nGREEN
	PIO1[4]	MII1_RXD[0]						RGMII
	PIO1[5]	MII1_RXD[1]						RGMII
	PIO1[6]	MII1_RXD[2]	KEY_SCAN_OUT[0]					RGMII
	PIO1[7]	MII1_RXD[3]	KEY_SCAN_OUT[1]					RGMII
SBC	**PIO2**	**MII1, RMII1, GMII1, RevMII1, HDMI**	**RMII1, Key scanning**	**UART11**	**GMII1**			
	PIO2[0]	MII1_RXDV						RGMII

Partition	PIO pins	Alternate 1	Alternate 2	Alternate 3	Alternate 4	Alternate 5	Alternate 6	4kOpen board allocation
	PIO2[1]	MII1_RXER						RGMII
	PIO2[2]	MII1_RXCLK						RGMII
	PIO2[3]	MII1_PHYCLK	MII1_PHYCLK		GMII1_GTXCLK			RGMII
	PIO2[4]	HDMI_CEC						HDMI_CEC
	PIO2[5]							PIO_EDID_notWP
	PIO2[6]		KEY_SCAN_IN[3]	UART11_TXD	MII1_TXD[4]			PIO2[6]
	PIO2[7]		KEY_SCAN_OUT[3]	UART11_RXD	MII1_TXD[5]			PIO2[7]
SBC	**PIO3**	**PWM10, UART10**	**SSC11, SSC12, ACG clk obs**	**UART11, EXT_IT[2]**	**GMII1**			
	PIO3[0]	PWM10_OUT	SSC11_MRST	UART11_CTS	MII1_RXD[4]			DVDD_1V0_AVS
	PIO3[1]	PWM10_COMPAREOUT	SSC11_MTSR	UART11_RTS	MII1_RXD[5]			PIO_PCIE_notINT
	PIO3[2]	PWM10_CAPTUREIN	SSC11_SCL	UART11_NOT_OE	MII1_RXD[6]			SBC_PWR_CTRL
	PIO3[3]	FP_RESETN		EXT_IT[2]	MII1_RXD[7]			PIO3[3]
	PIO3[4]	UART10_TXD	SSC12_MRST					PIO3[4] (UART10_TXD debug trace)
	PIO3[5]	UART10_RXD						PIO3[5] (UART10_RXD debug trace)
	PIO3[6]	UART10_CTS	SSC12_MTSR					PME (Ethernet waik-up)
	PIO3[7]	UART10_RTS	SSC12_SCL		MII1_CLK_125			M_RGMII1_CLK125
SBC	**PIO4**	**UART10, PWM11, SSC10**	**IRB10, CPUs debug, LPM_CLK**	**EXT_IT[3], rst obs output, PWM12, PWM13**	**GMII1, key scanning**	**LPM_CLK**	**key scanning**	
	PIO4[0]	UART10_NOT_OE	IRB10_IR_IN				KEY_SCAN_IN[0]	PIO4[0]
	PIO4[1]		IRB10_UHF_IN		MII1_TXD[6]		KEY_SCAN_IN[1]	PIO4[1]
	PIO4[2]	PWM11_COMPAREOUT	IRB10_IR_DATA_OUT		MII1_TXD[7]		KEY_SCAN_OUT[0]	PIO4[2]
	PIO4[3]	PWM11_CAPTUREIN		EXT_IT[3]	MII1_PHY_REF_CLK	LPM_CLK	KEY_SCAN_OUT[1]	PIO4[3]
	PIO4[4]	PWM11_OUT		SBC_OBS_NOTRST	KEY_SCAN_IN[0]			PIO4[4]
	PIO4[5]	SSC10_SCL			KEY_SCAN_IN[1]			PIO4[5]
	PIO4[6]	SSC10_MTSR		PWM12_OUT	KEY_SCAN_OUT[0]			PIO4[6]
	PIO4[7]	SSC10_MRST	LPM_EXT_OSC_CLK	PWM13_OUT	KEY_SCAN_OUT[1]			CPU_1V0_AVS
SBC	**PIO5**	**SSC11, HDMI Tx, HDMI Rx**			**key scanning**			
	PIO5[0]	SSC11_SCL						HDMI_TX_SCL
	PIO5[1]	SSC11_MTSR						HDMI_TX_SDA
	PIO5[2]				KEY_SCAN_OUT[2]			LMI_notRET_PIO
	PIO5[3]	HDMI_TX_HOT_PLUG						HDMI_TX
	PIO5[4]	HDMI_RX_HPD						HDMI_RX
	PIO5[5]	HDMI_RX_EDPD						HDMI_RX
	PIO5[6]	HDMI_RX_DDC_SDA						HDMI_RX
	PIO5[7]	HDMI_RX_DDC_SCL						HDMI_RX
FRONT	**PIO10**	**TSIN0 (s/p)**	**SSC0**	**MTSIN0 (p)**				
	PIO10[3]	TSIN0_BYTECLK		MTSIN0_BYTECLK				LCD_CS
FRONT	**PIO13**	**TSIN2 (s) TSIN3 (s)**	**TSIN2 (p), CA9 clk obs**	**SSC3, jitter clk obs**		**Denc CFC, Jitter clk obs**		
	PIO13[6]	TSIN3_VALID	TSIN2_DATA[5]	SSC3_MTSR				PIO13[6]
	PIO13[7]	TSIN3_PACKETCLK	TSIN2_DATA[4]	SSC3_MRST				PIO13[7]
FRONT	**PIO14**	**TSIN3 (s), SSC1, SSC2**	**TSIN2 (p), EXT_IT**	**TSIN4 (s)**				
	PIO14[2]	SSC1_SCL	TSIN2_DATA[1]	TSIN4_ERROR				PIO14[2]
	PIO14[3]	SSC1_MTSR	TSIN2_DATA[0]	TSIN4_VALID				PIO14[3]
	PIO14[4]	SSC1_MRST		TSIN4_PACKETCLK				PIO14[4]
	PIO14[5]	SSC2_SCL		TSIN4_BYTECLK				PIO14[5]
	PIO14[6]	SSC2_MTSR		TSIN4_DATA[7]				PIO14[6]
FRONT	**PIO15**	**UART2**	**NMI, SSC2**	**DVBCI**				
	PIO15[2]	UART2_CTS		DVBCI_ADDR[12]				LCD_RSTn
	PIO15[4]	UART2_NOT_OE	NMI	DVBCI_ADDR[10]				PIO15[4]
FRONT	**PIO16**	**UART1, SSC1**	**Smart Card 1**	**DVBCI**		**eMMC card**	**SD card**	
	PIO16[6]		SC1_C8_UART			EMMC_DATA[4]	SD_LED	PIO16[6]
	PIO16[7]		SC1_DETECT			EMMC_DATA[5]	SD_PWREN	PIO16[7]
FRONT	**PIO17**	**UART0, SSC3**	**Smart Card 0**	**MCHI**	**Clock Observation, Alt. PHY JTAG**			
	PIO17[0]	UART0_TXD	SC0_C4_UART		clockgen_d_13_obs_0			PIO17[0]
	PIO17[1]	UART0_RXD	SC0_C7_UART		clockgen_d_13_obs_1			PIO17[1]
	PIO17[2]	UART0_CTS	SC0_NOT_SET_VCC	MCHI_SCLK				PIO17[2]

Partition	PIO pins	Alternate 1	Alternate 2	Alternate 3	Alternate 4	Alternate 5	Alternate 6	4kOpen board allocation
	PIO17[3]	UART0_RTS	SC0_NOT_SET_VPP	MCHI_SCTL				PIO17[3]
	PIO17[6]	SSC3_SCL	SC0_C8_UART					LCD_SCL
	PIO17[7]	SSC3_MTSR	SC0_DETECT					LCD_SDI
FRONT	**PIO18**	**TSIN5 (s), SSC3**		**DVBCI**				
	PIO18[3]	TSIN5_BYTECLK		DVBCI_DATA[3]				FAN CTRL
FRONT	**PIO19**	**TSOUT1, SSC0**	**TSIN5 (s)**		**SSC1**	**eMMC/SD card**	**SD card**	
	PIO19[1]	TSOUT1_VALID	TSIN5_VALID	DVBCI_VS1N	SSC1_MTSR	EMMC_DATA[7]	SD_WP	LCDTS_RESET
	PIO19[2]	TSOUT1_PACKETCLK	TSIN5_PACKETCLK	DVBCI_RESET	SSC1_MRST	EMMC_SD_CMD		LCD_DISP
	PIO19[3]	TSOUT1_BYTECLK	TSIN5_BYTECLK	DVBCI_PWR1		EMMC_SD_CLK		LCDTS_INT
	PIO19[4]	TSOUT1_DATA[7]	TSIN5_DATA[7]	DVBCI_PWR2		EMMC_SD_DATA[0]		LCD_BL_CTRL
REAR	**PIO30**	**SSC4**	**DVO**	**RINGOSC debug**				
	PIO30[0]	SSC4_SCL	DVO0_HS					DVO_HS
	PIO30[1]	SSC4_MTSR	DVO0_VS					DVO_VS
	PIO30[2]	SSC4_MRST	DVO0_DE					DVO_DE
REAR	**PIO30[3]**		DVO0_CK					DVO_CK
	PIO30[4]		DVO0_D[0]					DVO_B[0]
	PIO30[5]		DVO0_D[1]					DVO_B[1]
	PIO30[6]		DVO0_D[2]					DVO_B[2]
	PIO30[7]		DVO0_D[3]					DVO_B[3]
REAR	**PIO31**	**PWM0, UART3**	**DVO**					
	PIO31[0]	PWM0_CAPTUREIN	DVO0_D[4]					DVO_B[4]
	PIO31[1]	PWM0_OUT	DVO0_D[5]					DVO_B[5]
	PIO31[2]	PWM0_COMPAREOUT	DVO0_D[6]					DVO_B[6]
REAR	**PIO31[3]**	UART3_TXD	DVO0_D[7]					DVO_B[7]
	PIO31[4]	UART3_RXD	DVO0_D[8]					DVO_G[0]
	PIO31[5]	UART3_CTS	DVO0_D[9]					DVO_G[1]
	PIO31[6]	UART3_RTS	DVO0_D[10]					DVO_G[2]
	PIO31[7]	UART3_NOT_OE	DVO0_D[11]					DVO_G[3]
REAR	**PIO32**	**External synchro, PCMIN0**	**DVO**					
	PIO32[0]	HSYNC	DVO0_D[12]					DVO_G[4]
	PIO32[1]	VSYNC	DVO0_D[13]					DVO_G[5]
	PIO32[2]		DVO0_D[14]					DVO_G[6]
REAR	**PIO32[3]**		DVO0_D[15]					DVO_G[7]
	PIO32[4]	AUDPCMIN0_DATA[0]	DVO0_D[16]					DVO_B[0]
	PIO32[5]	AUDPCMIN0_MCLK	DVO0_D[17]					DVO_B[1]
	PIO32[6]	AUDPCMIN0_SCLK	DVO0_D[18]					DVO_B[2]
	PIO32[7]	AUDPCMIN0_LRCLK	DVO0_D[19]					DVO_B[3]
REAR	**PIO33**	**PCMIN0, PCMOUT0**	**DVO, PCMIN0**	**Clock observation**				
	PIO33[0]	AUDPCMIN0_DATA[1]	DVO0_D[20]					DVO_B[4]
	PIO33[1]	AUDPCMIN0_DATA[2]	DVO0_D[21]					DVO_B[5]
	PIO33[2]	AUDPCMIN0_DATA[3]	DVO0_D[22]					DVO_B[6]
REAR	**PIO33[3]**		DVO0_D[23]					DVO_B[7]
	PIO33[4]	AUDPCMOUT0_DATA[0]						PIO33[4]
	PIO33[5]	AUDPCMOUT0_MCLK						PIO33[5]
	PIO33[6]	AUDPCMOUT0_SCLK	AUDPCMIN0_DATA[2]					PIO33[6]
	PIO33[7]	AUDPCMOUT0_LRCLK	AUDPCMIN0_DATA[3]					PIO33[7]
REAR	**PIO34**	**PCMOUT0, SSC5, EXT_IT, SPDIF**	**PCMIN0**	**SSC4, Clock observation**	**UART3**			
	PIO34[0]	AUDPCMOUT0_DATA[1]	AUDPCMIN0_MCLK	SSC4_SCL	UART3_TXD			PIO34[0]
	PIO34[1]	AUDPCMOUT0_DATA[2]	AUDPCMIN0_SCLK	SSC4_MTSR	UART3_RXD			PIO34[1]
	PIO34[2]	AUDPCMOUT0_DATA[3]	AUDPCMIN0_LRCLK	SSC4_MRST	UART3_CTS			PIO34[2]
REAR	**PIO34[3]**	SSC5_SCL						SSC5 (TC & PCIE SCL)
	PIO34[4]	SSC5_MTSR						SSC5 (TC & PCIE SDA)
	PIO34[5]							PCIE_PIO_RST
	PIO34[6]	EXT_IT[5]	AUDPCMIN0_DATA[0]		UART3_RTS			PIO34[6]
	PIO34[7]	AUDSPDIF_OUT	AUDPCMIN0_DATA[1]		UART3_NOT_OE			PIO34[7]
REAR	**PIO35**	**USB_A/B/C**	**SSC4 (I2C)**					
	PIO35[0]	USB_A_PRT_OVRCUR						USB0
	PIO35[1]	USB_A_PRT_PWR						MODE10
REAR	**PIO35[2]**	USB_B_PRT_OVRCUR						USB1
	PIO35[3]	USB_B_PRT_PWR						USB1
	PIO35[4]	USB_C_PRT_OVRCUR	SSC4_SCL					USB2

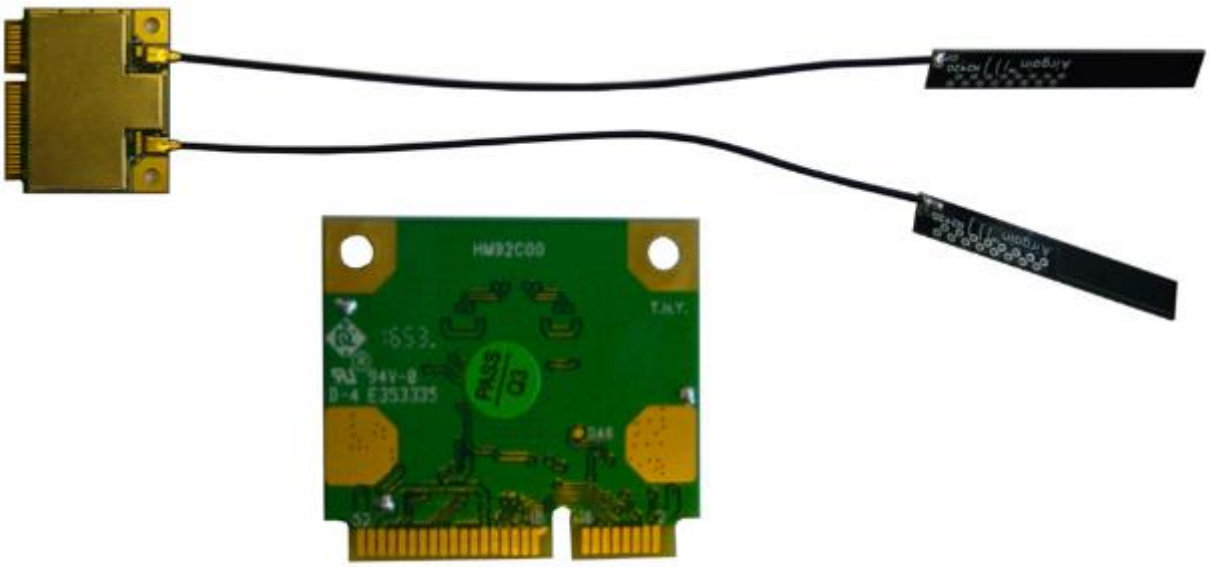
Partition	PIO pins	Alternate 1	Alternate 2	Alternate 3	Alternate 4	Alternate 5	Alternate 6	4kOpen board allocation
	PIO35[5]	USB_C_PRT_PWR	SSC4_MTSR					USB2
	PIO35[6]	USB_C_PRT_VBUS_VALID						USB2_VBUS_VALID
	PIO40	**SPI, eMMC**	**SD3.0**	**NAND Async**	**NAND Sync**			
	PIO40[0]	SPI_CSN_BOOT						SPI
	PIO40[1]	SPI_CLK						SPI
	PIO40[2]	SPI_DO						SPI
FLASH	**PIO40[3]**	SPI_DI						SPI
	PIO40[4]	SPI_WR_PROTECT		NANDa_CSN2	NANDs_CSN2			SPI
	PIO40[5]	SPI_HOLD		NANDa_CSN3	NANDs_CSN3			SPI
	PIO40[6]	EMMC_CLK	SD_CLK	NANDa_CSN1	NANDs_CSN1			SD_CLK
	PIO40[7]	EMMC_CMD	SD_CMD	NANDa_CSN0	NANDs_CSN0			SD_CMD
	PIO41	**eMMC**	**SD3.0**	**NAND Async**	**NAND Sync**			
	PIO41[0]	EMMC_D0	SD_DAT0	NANDa_DQ0	NANDs_DQ0			SD_DAT0
FLASH	**PIO41[1]**	EMMC_D1	SD_DAT1	NANDa_DQ1	NANDs_DQ1			SD_DAT1
	PIO41[2]	EMMC_D2	SD_DAT2	NANDa_DQ2	NANDs_DQ2			SD_DAT2
	PIO41[3]	EMMC_D3	SD_DAT3	NANDa_DQ3	NANDs_DQ3			SD_DAT3
	PIO42	**SPI**	**SD3.0**	**NAND Async**	**NAND Sync**			
FLASH	**PIO42[2]**		SD_PWREN	NANDa_ALE	NANDs_ALE			SD_PWREN
	PIO42[4]		SD_CD	NANDa_RNB	NANDs_RNB			SD_CD

GPIO connected to 40 pins GPIO connector
GPIO connected to 40 pins connector with multiple GPIO
GPIO used (and not connected to 40 pins GPIO connector)

5.6 WiFi Mini PCIe Module

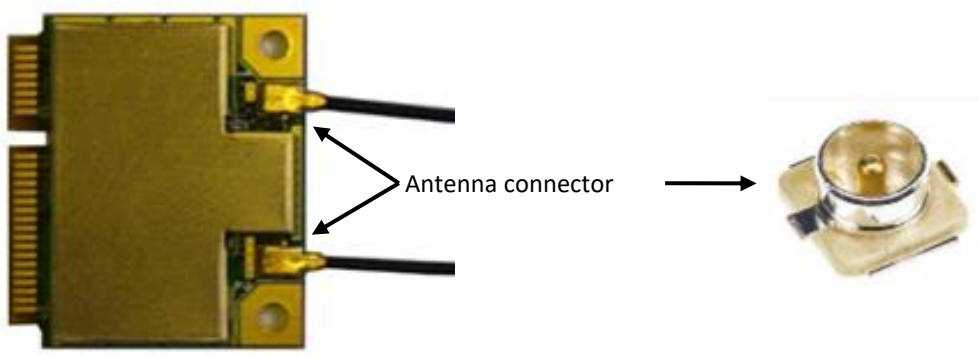
The default module assembled with the board is a WiFi Mini PCIe module with Realtek RTL8192EE-CG device 11n 2T2R minicard (Mini PCIe) 2x2 MIMO 802.11 b/g/n 2.4GHz

Figure 24: WiFi Mini PCIe module with antenna



There are two antenna 2.4-2.49 GHz to plug on U.FL Connector on WiFi module

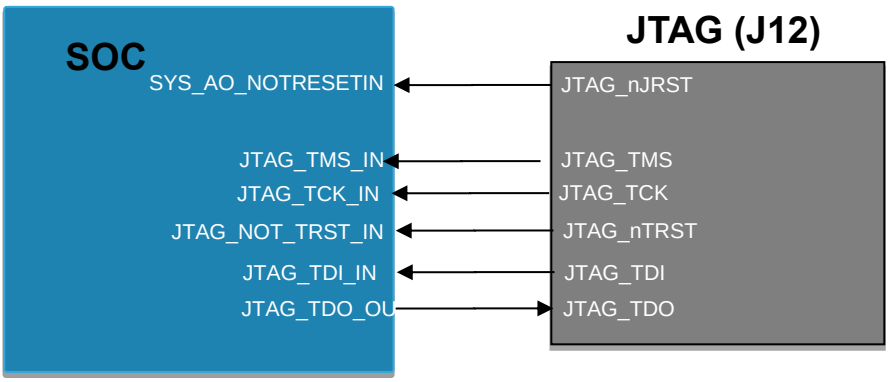
Figure 25: Antenna connectors



5.7 JTAG Debug Interface

The JTAG interface allows debug access.

Figure 26: JTAG to STiH418 connections



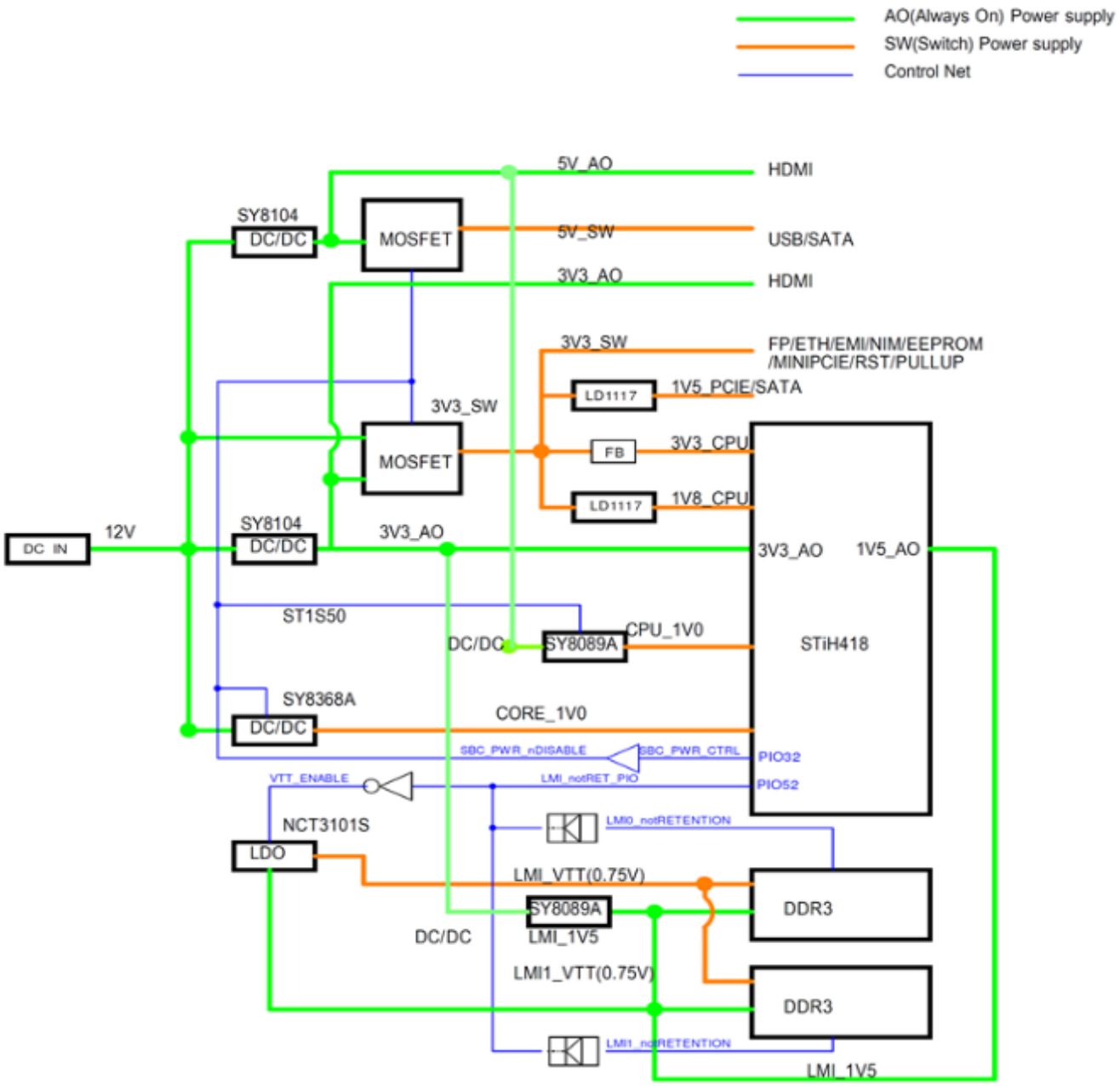
5.8 Power

The board is powered from a single +12V input (jack connector).

5.8.1 Power tree

All power supplies needed are derivate on board with dedicated DC/DC solution from +12V.

Figure 27: Board power tree



The board can deliver up to 500mA on 3V3 supply of the 40 pins GPIO connector.

5.8.2 External Power plug

Figure 28: power plug kit

5.9 PCB Characteristics

Table 19: PCB characteristics

Parameter	Details
Copper layers	4 layers
Material	IT-158
TG level	TG150
PCB size	100mm x 100mm
Minimum track width	0,1 mm
Minimum track spacing	0,1 mm
Minimum hole size Drill diameter / antipad	0.25mm / 0,65mm
Minimum Solder resist registration	50µ
Minimum solder resist width	80µ
PCB thickness:	1,6 mm

Table 20: PCB stacking

		Thickness		Dielectric Constant
		(um)	mils	
	top solder resist	25.40	1.00	3.2 @ 1 MHz
Layer 1	copper	35.00	1.38	
	dielectric IT-180A 3313	95.00	3.74	3.9 or 4.24
Layer 2	copper	35.00	1.38	
	dielectric IT-180A 3313	1230.00	48.43	3.9 or 4.24
Layer 3	copper	35.00	1.38	
	dielectric IT-180A 3313	95.00	3.74	3.9 or 4.24
Layer 4	copper	35.00	1.38	
	bottom solder resist	25.40	1.00	3.2 @ 1 MHz
	Total	1610.80	63.42	

Track impedance control are between L1/L2 and L3/L4

Table 21: Track impedance

Items	Impedance Target	Trace		Impedance Simulated	
		W1 - width (um)	S1 - separation (um)	Er1= 4,1	Er1= 4,4
DDR, PCIE	diff 100 ohm +/- 10 ohms	100	100	93	91
SATA, IFE Serdes	diff 100 ohm +/- 10 ohms loosely coupled	130	180	96	94
DDR	single ended 55 ohm +/- 10 ohms	100	NA	60	58

6 Package and kit delivery

The 4kOpen HW package kits contains:

- 4kOpen B2264 board
- WiFi 2.4GHz Mini PCIe module 2X2 plug on the Mini PCIe connector
- 2 * WiFi patch antenna 2.4GHz
- Power plug AC to DC +12V

Figure 29: 4kOpen HW package kit

7 Application: How to add an infrared receiver

This section describes how to add an infrared receiver for remote control.

The example is based on an IR reference RPM7238-H5 from Rohm for Remote Control Systems, 3V3 with sub carrier frequency = 37.9kHz.

Figure 30: Infrared Receiver schematics

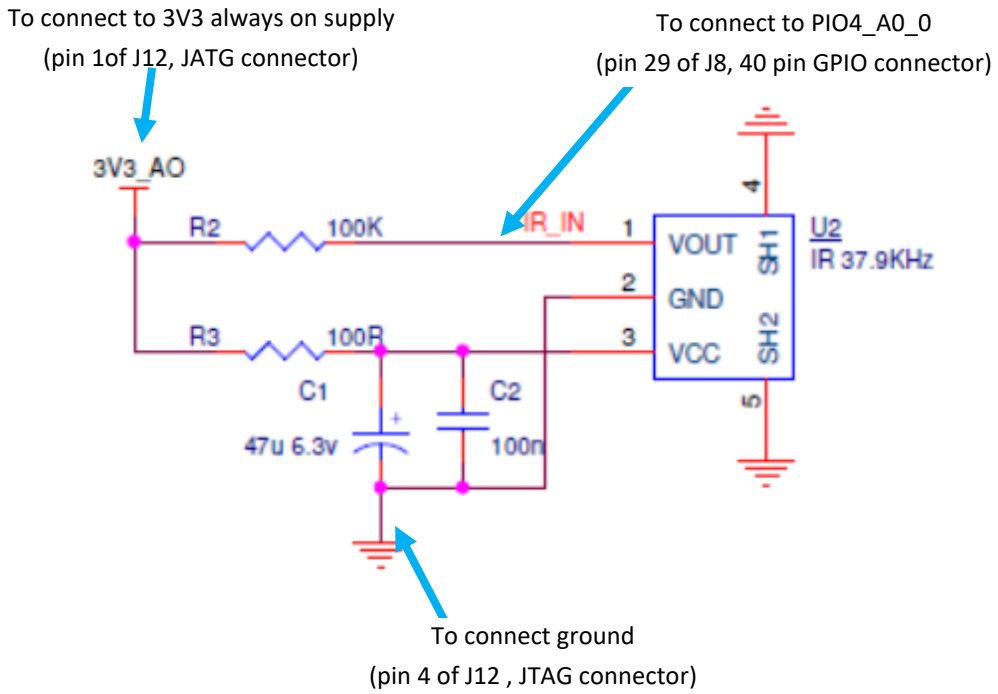
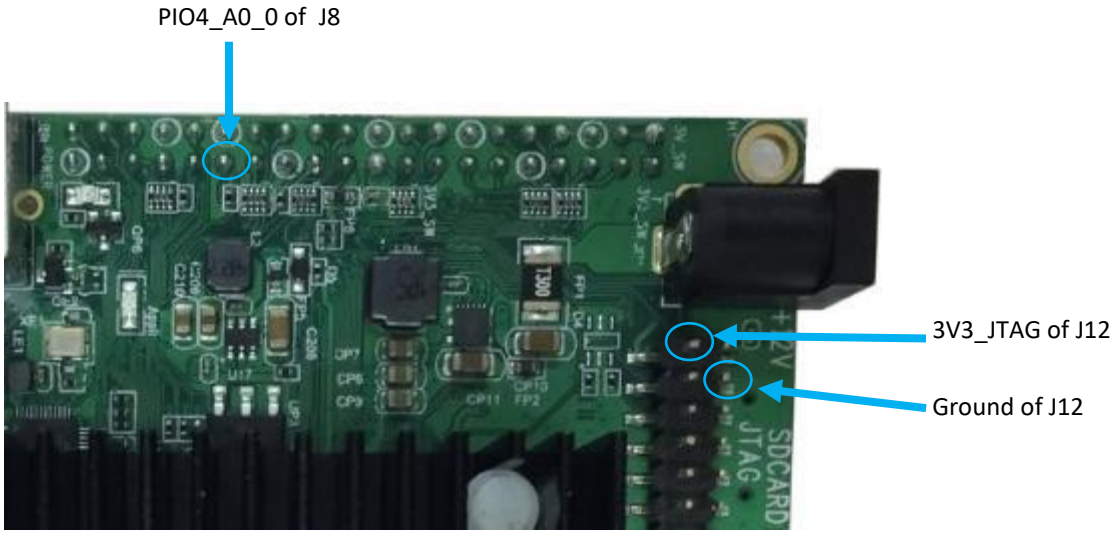


Figure 31: Infrared Receiver implementation



8 Revision history

Table 22: Document revision history

Date	Revision	Changes
24th Jan 2018	Release 1.0	Initial version
26th Feb 2018	Release 1.1	Revised branding
28th February 2018	Release 1.2	Update Table 18: SOC GPIO
6th November 2018	Release 1.3	Minor Fixes